PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-198505

(43)Date of publication of application : 12.07.2002

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(51)Int.Cl. H01L 27/146
H04N 5/335

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(54) SOLID-STATE IMAGE PICKUP DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the occurrence of a trouble, such as smear, sensitivity deterioration, etc., caused by oblique incident light in a solid-state image pickup device.

SOLUTION: The solid-state image pickup device is provided with a plurality of picture elements. In the device, two photodiodes 1 and 40 are formed against each picture element. Two light entrance openings 24a and 24b are formed in each light shield film 24 correspondingly to the photodiodes 1 and 40. Oblique light reflecting sections 60-62 which partially reflect the light obliquely made incident to the device through the openings 24a and 24b are partially foamed along the whole circumferences of the openings 24a and 24b at height positions between the photodiodes 1 and 40 and oblique light reflecting films 24.

LEGAL STATUS [Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]

[Claim 1] In the solid state camera which has the light-shielding film which it has two or more pixels, and one or more light sensing portions are formed to said each pixel, and has opening for optical incidence to said one or more light sensing portions About each of all or a part of pixels of said two or more pixels, a part of perimeter [at least] of said opening corresponding to at least one of said one or more light sensing portions corresponding to the pixel concerned is met. The solid state camera characterized by forming the oblique light reflective section which reflects a part of oblique light which is the light which carries out incidence aslant from the opening concerned in the height location between at least one light sensing portion and said light-shielding films concerned.

[Claim 2] Said oblique light reflective section is a solid state camera according to claim 1 characterized by being formed along with the whole substantially [said perimeter].

[Claim 3] Said oblique light reflective section is a solid state camera according to claim 1 or 2 characterized by the side face of said reflecting layer reflecting said

a part of oblique light including the reflecting layer which consisted of same ingredients as the electrode layer or wiring layer located in a downward height location to said light-shielding film.

[Claim 4] Said a part of oblique light reflective section [at least] is the solid state camera according to claim 1 to 3 characterized by being used also [wiring layer / which is located in a downward height location to said light-shielding film / the electrode layer or wiring layer].

[Claim 5] Said oblique light reflective section is a solid state camera according to claim 1 to 3 characterized by having dissociated with the electrode layer or wiring layer located in a downward height location to said light-shielding film, and being formed.

[Claim 6] Said a part of oblique light reflective section [at least] is the solid state camera according to claim 1 to 5 characterized by forming through hole structure.

[Claim 7] Said oblique light reflective section is a solid state camera according to claim 1 to 6 characterized by having been arranged so that it may become **** point symmetry centering on the center position of said opening corresponding to the oblique light reflective section concerned.

[Claim 8] Said oblique light reflective section responds to the location of the pixel

corresponding to the oblique light reflective section concerned. Arrangement of the oblique light reflective section concerned to said opening corresponding to said oblique light reflective section corresponding to at least one of the pixels which arrangement of the oblique light reflective section concerned to said opening corresponding to the oblique light reflective section concerned is defined, and is said two or more pixels, The solid state camera according to claim 1 to 6 with which arrangement of the oblique light reflective section concerned to said opening corresponding to said oblique light reflective section corresponding to other at least one pixels of said two or more pixels is characterized by differing.

[Claim 9] Two or more photoelectrical converters in which it is two or more photoelectrical converters arranged in the shape of two-dimensional, and each generates and accumulates the signal charge according to incident light, Two or more amplifiers which it is two or more amplifiers prepared corresponding to said two or more photoelectrical converters, and each has regulatory region, and produce the signal output according to the charge of this regulatory region, Two or more transfer sections which are two or more transfer sections prepared corresponding to said two or more photoelectrical converters, and transmit the

signal charge which was generated, respectively and was accumulated by said two or more photoelectrical converters to said regulatory region of two or more of said amplifiers, respectively, Two or more wiring with which each was prepared for every line of two or more of said photoelectrical converters, and two or more semiconductor regions prepared corresponding to said two or more amplifiers, They are two or more switching elements which are prepared for every line of two or more of said photoelectrical converters, and control the electric connection and the cutoff between said two or more semiconductor regions corresponding to the line concerned, and said regulatory region of two or more of said amplifiers corresponding to the line concerned. Two or more switching elements to which each makes said regulatory region of either of the semiconductor regions of said plurality corresponding to the line concerned, and either of said two or more amplifiers corresponding to the line concerned a main-electrode field, respectively, A preparation and at least one semiconductor region of two or more of said whole semiconductor regions When it is formed so that the signal charge according to incident light may be generated, and said two or more switching elements corresponding to the line concerned are in switch-on for every line of two or more of said photoelectrical converters While being in the

condition that said regulatory region of two or more of said amplifiers corresponding to the line concerned was electrically connected to said wiring corresponding to the line concerned When said two or more switching elements corresponding to the line concerned are in a cut off state It will be in the condition that said regulatory region of two or more of said amplifiers corresponding to the line concerned was electrically intercepted to said wiring corresponding to the line concerned. About each line to which said at least one semiconductor region relates among the lines of two or more of said photoelectrical converters When said two or more switching elements corresponding to the line concerned are in switch-on Said at least one semiconductor region will be in the condition of having connected electrically to said wiring corresponding to the line concerned. Said photoelectrical converter constitutes one of said one or more light sensing portions formed to said pixel. The solid state camera according to claim 1 to 8 characterized by what said at least one semiconductor region formed so that the signal charge according to said incident light might be generated constitutes other one of said said one or more light sensing portions formed to said pixel for.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to a solid state camera.

[0002]

[Description of the Prior Art] Conventionally, solid state cameras, such as CCD,

CMOS image sensors, and magnification mold image sensors, are offered as an image input component of an electronic camera.

[0003] In such conventional various solid state cameras, it has two or more pixels, one or more light sensing portions are formed to said each pixel, and it has the light-shielding film with opening for optical incidence to said one or more light sensing portions.

[0004]

[Problem(s) to be Solved by the Invention] However, in the conventional solid state camera, it did not have the structure considered about the oblique light which is the light which carries out incidence aslant from opening of said light-shielding film, but when a part of oblique light also reached the part around a light sensing portion, various inconvenience had arisen. Generating of a smear, lowering of sensibility, etc. can be mentioned as an example of such inconvenience. moreover, if other examples of said inconvenience are explained, for example like the solid state camera currently indicated by JP,11-204769,A etc. In the solid state camera equipped also with the light sensing portion for the amount monitors of incident light besides the light sensing portion for an image pick-up which receives original incident light in order to acquire a video signal

The optical generating charge produced from opening corresponding to the light sensing portion for an image pick-up according to a part of oblique light which carried out incidence mixed to the optical generating charge which should be essentially obtained from the light sensing portion for the amount monitors of incident light, and there was a case where it became impossible for precision to improve the amount of incident light a monitor. The inconvenience explained above becomes remarkable as the consistency of a light sensing portion increases by raising the degree of integration of a pixel or preparing two or more light sensing portions to one pixel.

[0005] This invention was made in view of such a situation, and aims at offering the solid state camera which can reduce the inconvenience accompanying the oblique light which carries out incidence.

[0006]

[Means for Solving the Problem] In order to solve said technical problem, the solid state camera by the 1st mode of this invention In the solid state camera which has the light-shielding film which it has two or more pixels, and one or more light sensing portions are formed to said each pixel, and has opening for optical incidence to said one or more light sensing portions About each of all or a

part of pixels of said two or more pixels, a part of perimeter [at least] of said opening corresponding to at least one of said one or more light sensing portions corresponding to the pixel concerned is met (the thing of the perimeter met 30% or more is desirable). the thing of the perimeter met 50% or more is more desirable, and the thing of the perimeter met 70% or more is much more desirable. In the height location between at least one light sensing portion and said light-shielding films concerned, the oblique light reflective section which reflects a part of oblique light which is the light which carries out incidence aslant from the opening concerned is formed.

[0007] According to this 1st mode, since the oblique light reflective section is formed, it is reflected in the oblique light reflective section, and a part of oblique light carries out incidence to a light sensing portion. Therefore, while the amount of the oblique light which carries out incidence to the part around a light sensing portion is reduced, the quantity of light which carries out incidence to a light sensing portion increases, and sensibility increases. Consequently, the inconvenience accompanying the oblique light which carries out incidence is reduced. For example, a smear is reduced, sensibility increases and the monitor precision of the amount of incident light increases depending on the case.

[0008] In addition, in said 1st mode, although the oblique light reflective section may be formed about two or more pixels, the oblique light reflective section may be formed only about the pixel by the side of the circumference of the field over which said two or more pixels are distributed, for example. While the light which does not almost have an inclination carries out incidence to the pixel near the core of said field since the optical axis of an image formation lens is set up near the core of said field when this carries the solid state camera concerned in an electronic camera, for example, since the distance from the optical axis of said lens becomes large, in the pixel by the side of the circumference, it is because the inclination of the light which carries out incidence becomes large.

[0009] In said 1st mode, as for the solid state camera by the 2nd mode of this invention, said oblique light reflective section is formed along with the whole substantially [said perimeter].

[0010] In this 2nd mode, since the oblique light reflective section is formed along with the whole substantially [said perimeter], while being able to reduce further the amount of the oblique light which carries out incidence to the part around a light sensing portion, the quantity of light which carries out incidence to a light sensing portion increases more, sensibility increases further, and it is desirable

irrespective of the sense of an oblique light.

[0011] the 3rd voice of this invention -- the solid state camera twisted like -- said 1st or 2nd voice -- it sets like and the side face of said reflecting layer reflects said a part of oblique light including the reflecting layer which consisted of ingredients as the electrode layer or wiring layer located in a downward height location to said light-shielding film with said same oblique light reflective section.

[0012] Since the ingredient of the reflecting layer which constitutes a part of oblique light reflective section [at least] consists of same ingredients (for example, ingredient which uses aluminum as a principal component) as said electrode layer or wiring layer according to this 3rd mode, on the occasion of manufacture of the solid state camera concerned, said wiring layer can be formed by the same production process as said electrode layer or wiring layer. For this reason, the oblique light reflective section can be formed easily and a cost cut can be aimed at.

[0013] the 4th voice of this invention -- the solid state camera twisted like -- said voice of either the 1st thru/or the 3rd either -- it sets like and said a part of oblique light reflective section [at least] is used also [wiring layer / which is located in a downward height location to said light-shielding film / the electrode

layer or wiring layer].

[0014] According to this 4th mode, since a part of oblique light reflective section [at least] is used also [wiring layer / said / electrode layer or wiring layer], structure becomes easy and a cost cut can be aimed at.

[0015] In said mode of either the 1st thru/or the 3rd either, said oblique light reflective section separates the solid state camera by the 5th mode of this invention with the electrode layer or wiring layer located in a downward height location to said light-shielding film, and it is formed.

[0016] In said the 1st thru/or 3rd mode, like said 4th mode, although a part of oblique light reflective section [at least] may be used also [wiring layer / said / electrode layer or wiring layer], the oblique light reflective section may be separated with said electrode layer or wiring layer like said 5th mode.

[0017] In the solid state camera by the 6th mode of this invention, in said mode of either the 1st thru/or the 5th either, said a part of oblique light reflective section [at least] forms through hole structure. Here, although through hole structure means the same structure as a through hole, any are sufficient as the existence of the function of electrical installation.

[0018] Since through hole structure is adopted according to this 6th mode, the

area of the effective reflector in the oblique light reflective section can be increased, the amount of echoes to an oblique light can be increased, the quantity of light which carries out incidence to a light sensing portion while being able to reduce further the amount of the oblique light which carries out incidence to the part around a light sensing portion increases more, sensibility increases further, and it is desirable. Moreover, on the occasion of manufacture of the solid state camera concerned, the through hole structure of the oblique light reflective section can also be formed by the same production process as the through hole about the electrode layer or wiring layer located in a downward height location to a light-shielding film. For this reason, the oblique light reflective section can be formed easily and a cost cut can be aimed at.

[0019] the 7th voice of this invention -- the solid state camera twisted like -- said voice of either the 1st thru/or the 6th either -- it sets like, and said oblique light reflective section is arranged so that it may become **** point symmetry centering on the center position of said opening corresponding to the oblique light reflective section concerned.

[0020] Although the sense of the oblique light which carries out incidence to opening according to the location of a pixel differs, if the oblique light reflective

section is arranged like said 7th mode so that it may become **** point symmetry, dispersion in the reflection property (the amount of echoes of the oblique light reflective section) of the oblique light reflective section by the location of a pixel can be reduced, and it is desirable. And since it becomes possible to make the same arrangement to opening of the oblique light reflective section also about which pixel according to said 7th mode, a pattern design etc. becomes easy.

[0021] The solid state camera by the 8th mode of this invention is set in said mode of either the 1st thru/or the 6th either. The (a) aforementioned oblique light reflective section According to the location of the pixel corresponding to the oblique light reflective section concerned, arrangement of the oblique light reflective section concerned to said opening corresponding to the oblique light reflective section concerned is defined. (b) Arrangement of the oblique light reflective section concerned to said opening corresponding to said oblique light reflective section corresponding to at least one pixel in said two or more pixels, Arrangement of the oblique light reflective section concerned to said opening corresponding to said oblique light reflective section corresponding to other at least one pixels of said two or more pixels differs.

[0022] By this 8th mode as well as said 7th mode, dispersion in the reflection

property (the amount of echoes of the oblique light reflective section) of the oblique light reflective section by the location of a pixel can be reduced, and it is desirable.

[0023] The solid state camera by the 9th mode of this invention is set in said mode of either the 1st thru/or the 8th either. Two or more photoelectrical converters in which it is two or more photoelectrical converters arranged in the shape of two-dimensional, and each generates and accumulates the signal charge according to incident light, Two or more amplifiers which it is two or more amplifiers prepared corresponding to said two or more photoelectrical converters, and each has regulatory region, and produce the signal output according to the charge of this regulatory region, Two or more transfer sections which are two or more transfer sections prepared corresponding to said two or more photoelectrical converters, and transmit the signal charge which was generated, respectively and was accumulated by said two or more photoelectrical converters to said regulatory region of two or more of said amplifiers, respectively, Two or more wiring with which each was prepared for every line of two or more of said photoelectrical converters, and two or more semiconductor regions prepared corresponding to said two or more amplifiers, They are two or

more switching elements which are prepared for every line of two or more of said photoelectrical converters, and control the electric connection and the cutoff between said two or more semiconductor regions corresponding to the line concerned, and said regulatory region of two or more of said amplifiers corresponding to the line concerned. Two or more switching elements to which each makes said regulatory region of either of the semiconductor regions of said plurality corresponding to the line concerned, and either of said two or more amplifiers corresponding to the line concerned a main-electrode field, respectively, A preparation and at least one semiconductor region of the whole semiconductor region of the (a) aforementioned plurality When it is formed so that the signal charge according to incident light may be generated, and said two or more switching elements corresponding to the line concerned are in switch-on for every line of the photoelectrical converter of the (b) aforementioned plurality While being in the condition that said regulatory region of two or more of said amplifiers corresponding to the line concerned was electrically connected to said wiring corresponding to the line concerned When said two or more switching elements corresponding to the line concerned are in a cut off state It will be in the condition that said regulatory region of two or more of said amplifiers

corresponding to the line concerned was electrically intercepted to said wiring corresponding to the line concerned. (c) about each line to which said at least one semiconductor region relates among the lines of two or more of said photoelectrical converters When said two or more switching elements corresponding to the line concerned are in switch-on Said at least one semiconductor region will be in the condition of having connected electrically to said wiring corresponding to the line concerned. (d) Said photoelectrical converter constitutes one of said one or more light sensing portions formed to said pixel. (e) Said at least one semiconductor region formed so that the signal charge according to said incident light might be generated constitutes other one of said said one or more light sensing portions formed to said pixel.

[0024] This 9th mode is the example applied to the solid state camera equipped also with the light sensing portion for the amount monitors of incident light (said semiconductor region) besides the light sensing portion for an image pick-up (said photoelectrical converter) which receives incident light original for an image pick-up which was indicated by JP,11-204769,A in said the 1st thru/or 8th mode. According to this 9th mode, it also becomes possible to, acquire the effectiveness of precision being able to improve the amount of incident light a

monitor for example.

[0025]

[Embodiment of the Invention] Hereafter, the solid state camera by this invention is explained with reference to a drawing.

[0026] [The gestalt of the 1st operation]

[0027] Drawing 1 is the outline top view showing typically the unit pixel of the solid state camera by the gestalt of operation of the 1st of this invention. Drawing 2 is the outline sectional view which met X1-X2 line in drawing 1 . Drawing 3 is the outline sectional view which met Y1-Y2 line in drawing 1 . Drawing 4 is the outline sectional view which met Y3-Y4 line in drawing 1 . Drawing 5 is the circuit diagram showing the equal circuit of this unit pixel.

[0028] The solid state camera by the gestalt of this operation has the configuration with which the unit pixel shown in drawing 1 thru/or drawing 5 was arranged by the two-dimensional matrix (mxn). The photodiode 1 as a photoelectrical converter which generates and accumulates the signal charge according to incident light as this unit pixel is shown in drawing 1 thru/or drawing 5 , The junction field effect transistor 2 as an amplifier which produces the signal output (magnification output) according to the charge of the gate field 15 as

regulatory region (henceforth "JFET"), The transfer gate 3 which consists of polish recon as the transfer section which transmits the signal charge generated and accumulated with the photodiode 1 to the gate field 15 of JFET2, The reset drain wiring 24 as wiring with which driving signal phiRSD for controlling the potential of the gate field 15 concerned while making the charge of the gate field 15 of JFET2 discharge is supplied, The reset drain 4 as a P type diffusion layer (P-type semiconductor field) established corresponding to JFET2, It is P channel MOSFET9 which is an insulated-gate mold transistor as a switching element which controls the electric connection and the cutoff between this reset drain 4 and the gate field 15 of JFET2. While making the reset drain 4 of the pixel concerned, and the gate field 15 of JFET2 of the pixel concerned into a main-electrode field, respectively, it has P channel MOSFET9 which uses a reset gate 5 as a control electrode.

[0029] Said photodiode 1, JFET2, and the reset drain 4 are formed into the low concentration N type epitaxial layer 11 formed in the main front-face side upper part of the N type high concentration silicon substrate 10, and the transfer gate 3 and a reset gate 5 are formed through the insulator layer 33 on the N type epitaxial layer 11.

[0030] As shown in drawing 3 and drawing 4 , a photodiode 1 consists of a P type charge storage field 12 formed into the N type epitaxial layer 11, a high-concentration N-type semiconductor field 13 formed near the semi-conductor front face of the P type charge storage field 12 upper part, and an N type epitaxial layer 11, and is the photodiode of a flush type.

[0031] The gate field 15 which consists of a P type diffusion layer formed into the N type epitaxial layer 11 as JFET2 is shown in drawing 2 and drawing 3 , The high-concentration N type source field 14 and the high-concentration N type channel field 17 which were formed all over this P type gate field 15, It consists of drain fields which consist of a part of the N type epitaxial layer 11 of the location which faces the source field 14 across the channel field 17, and in the gate field 15, reception and this are amplified and the charge of a photodiode 1 is outputted.

[0032] As shown in drawing 1 , drawing 3 , and drawing 4 , the high-concentration N type diffusion layer 16 used as the isolation region between the pixels which adjoin mutually is continuously formed in the perimeter field of a pixel with the N type source field 14 and the N type epitaxial layer 11 which constitute a photodiode 1. Therefore, the N type field (11 13) of the PN

junction which constitutes a photodiode 1, and the N type drain field (a part of N type epitaxial layer 11) of JFET are connected electrically.

[0033] The P type gate field 15 of JFET2 is formed so that it may face across the N type channel field 17 from the upper and lower sides, it suppresses the substrate bias effectiveness, and it has structure which oppresses gain dispersion at the same time it raises the gain of source follower actuation.

[0034] As shown in drawing 3 , the transfer gate 3 consists of gate electrodes formed through the insulator layer 33 on the border area of the P type charge storage field 12 of a photodiode 1, and the P type gate field 15 of JFET2, and transmits the charge accumulated in the P type charge storage field 12 of a photodiode 1 to the P type gate field 15 of JFET2.

[0035] That is, P channel MOSFET consists of a P type field (P type charge storage field 12) of the PN junction which constitutes a photodiode 1, the transfer gate 3, and a P type gate field 15 of JFET2.

[0036] To be shown in drawing 2 and drawing 4 , the reset drain 4 consists of P-type semiconductor fields formed into the N type epitaxial layer 11, and discharges the charge which generation are recording was carried out with the photodiode 1, and was transmitted to the P type gate field 15 of JFET2, and

controls the potential of the P type gate field 15 of JFET2 through a reset gate 5 (namely, P channel MOSFET9 which has a reset gate 5).

[0037] To be shown in drawing 2 , a reset gate 5 consists of gate electrodes formed through the insulator layer 33 on the border area with the reset drain 4 which is the P type gate field 15 and P-type semiconductor field of JFET2, and controls the electric connection condition of the P type gate field 15 of JFET2, and the reset drain 4. That is, as mentioned above, P channel MOSFET9 consists of the P type gate fields 15, the reset gates 5, and the reset drains 4 of JFET2. In addition, this MOSFET9 is using the reset gate 5 as the control electrode while making the reset drain 4 of the pixel concerned, and the gate field 15 of JFET2 of the pixel concerned a main-electrode field, respectively.

[0038] Moreover, on the border area of the P type gate field 15 of JFET2 of the pixel concerned, and the reset drain 4 of the contiguity pixel of one side of a line writing direction, gate electrode (drawing 1 and gate electrode of left-hand side in drawing 2) 5a is formed through the insulator layer 33. Moreover, on the border area of the reset drain 4 of the pixel concerned, and the P type gate field 15 of JFET2 of the contiguity pixel of the other side of a line writing direction, gate electrode (drawing 1 and gate electrode of right-hand side in drawing 2) 5a

is formed through the insulator layer 33. that is If the P type gate field 15 of JFET2 of the pixel concerned and the reset drain 4 of the contiguity pixel of one side of a line writing direction are made into a main-electrode field, respectively Drawing 1 as a switching element between the pixels which both use gate electrode 5a of the left-hand side in drawing 1 as a control electrode, and P channelMOSFET9a of the left-hand side in drawing 2 , It reaches. If the reset drain 4 of the pixel concerned and the P type gate field 15 of JFET2 of the contiguity pixel of the other side of a line writing direction are made into a main-electrode field, respectively P channel MOSFET9a of drawing 1 as a switching element between the pixels which both use gate electrode 5a of the right-hand side in drawing 1 as a control electrode, and the right-hand side in drawing 2 is formed. The gate electrodes 5a and 5a are continuously formed of polish recon with the reset gate wiring 21 as well as the reset gate 5, and the gate electrodes 5a and 5a and a reset gate 5 are connected in common by the reset gate wiring 21 concerned.

[0039] Furthermore, the overflow control field 6 which leads the charge superfluously generated with the photodiode 1 to the reset drain 4 is formed. The overflow control field 6 consists of a P-type semiconductor field formed in the N

type epitaxial layer 11 interior of the P type charge storage field 12 of a photodiode 1, and a border area with the reset drain 4, and controls the overflow actuation which leads the charge superfluously generated with the photodiode 1 to the reset drain 4. Moreover, near the semi-conductor front face of the overflow control field 6 upper part, the high-concentration N-type semiconductor field 16 mentioned above is formed. That is, P channel JFET which made the P type charge storage field 12 of a photodiode 1, the P type overflow control field 6, and the reset drain 4 the source field, the channel field, and the drain field, respectively, and made the gate field the high-concentration N-type semiconductor field 16 and the high-concentration N type epitaxial layer 11 is formed. This P channel JFET is in a cut-off (cutoff) condition, when the photodiode 1 is carrying out standard actuation, a light strong against a photodiode 1 carries out incidence, and if the charge more than the constant rate in the P type charge storage field 12 (in this case, positive charge by the hole) is accumulated (i.e., if it goes up more than level with the potential of the P type charge storage field 12), it is formed so that it may be in a flow (ON) condition. Therefore, the charge generated superfluously flows into the reset drain 4 via the overflow control field 6 with a photodiode 1. This superfluous charge is

discharged from the reset drain wiring 24 via a predetermined path. The high-concentration N-type semiconductor field 16 formed near the semi-conductor front face of the overflow control field 6 upper part is continuously formed with the high-concentration N-type semiconductor field 13 formed near the front face of a photodiode 1. Therefore, it becomes the structure covered in the high-concentration N-type semiconductor field (13 and 16) near the semi-conductor front face of the P type charge storage field 12 of a photodiode 1 also including a perimeter field, and the photodiode 1 is an embedding photodiode. In addition, although the high-concentration N-type semiconductor field (13 and 16) is not formed in the edge by the side of the transfer gate 3 of a photodiode 1, and the transfer gate 3 lower part on structure, the engine performance (low dark current property by depletion[non-]-izing on the front face of a semi-conductor) of an embedding photodiode is held. During the period when, as for this, the photodiode 1 is performing are recording actuation of a signal charge by photo electric translation, the transfer gate 3 is in a cutoff (off) condition, and it is because the high-level pulse voltage is impressed, induction of the electron is carried out near the semi-conductor front face of this field as a result and it considers as a high-concentration N-type

semiconductor field. Thus, since the depletion layer produced in the PN-junction section does not arrive at a semi-conductor front face with an embedding photodiode while the photodiode 1 is the photodiode of the embedding mold equipped with the horizontal-type overflow drain structure of a JFET mold and being able to oppress the phenomenon of blots, such as a blooming and a smear, according to overflow structure, the dark current is oppressed. Moreover, in order that a charge may not remain in a photodiode after a charge is transmitted (based on a full transfer or perfect depletion-ization), an after-image and the ideal property which stopped the reset noise are acquired.

[0040] In addition, it is formed as the transfer gate wiring 20 which consists of polish recon, the reset gate wiring 21 which consists of polish recon, the reset drain wiring 24 which consists of 2nd layer aluminum film and which was mentioned above, and the vertical signal line (source wiring of JFET2) 22 by the 1st layer aluminum film are also shown in drawing. Namely, the N type source field 14 of each JFET2 is connected in common in the direction of a vertical scanning (the direction of a train) by the vertical signal line 22 for every train. Moreover, the reset gate 5 is connected in common in the direction of a horizontal scanning (line writing direction) for the transfer gate 3 by the transfer

gate wiring 20 the whole line with the reset gate wiring 21, respectively.

[0041] With the gestalt of this operation, the reset drain wiring 24 is made to serve a double purpose as a light-shielding film. While opening 24a for optical incidence is formed in the field corresponding to a photodiode 1, opening 24b for optical incidence is formed in the field corresponding to the reset drain 4 at the reset drain wiring 24. The reset drain wiring 24 as a light-shielding film is shading a bonnet and this field for the field except a photodiode 1 and the reset drain 4. In addition, although the reset drain wiring 24 is not shown in a drawing, it is electrically connected to the reset drain 4 of any one or more horizontal pixels for every line.

[0042] As mentioned above, it is a P-type semiconductor field, the N-type semiconductor field (N type epitaxial layer) 11 is arranged under this, and since the reverse bias of the reset drain 4 and the N-type semiconductor field 11 is always carried out (VDD>phi RSD), the reset drain 4 commits the reset drain 4 as photodiode 40 with the another photodiode 1 as a photoelectrical converter. In this photodiode 40, the photocurrent by the signal charge (this example hole) generated according to the light which carried out incidence to opening 24b occurs. That is, with the gestalt of this operation, the reset drain 4 as a

semiconductor region is formed so that the signal charge according to incident light may be generated. Thus, with the gestalt of this operation, to one pixel, in order to acquire a video signal, the photodiode 40 as a light sensing portion for the amount monitors of incident light is also formed besides the photodiode 1 as a light sensing portion for an image pick-up which receives original incident light.

[0043] And with the gestalt of this operation, as shown in drawing 1 and drawing 4 , in between a photodiode 1 and photodiodes 40, the oblique light reflective film 60 which consists of 1st layer aluminum film is formed in the height location between photodiodes 1 and 40 and a light-shielding film (reset drain wiring) 24. The both-sides side of the oblique light reflective film 60 meets a part of perimeter of opening 24a (it corresponds to a photodiode 1) of the wiring 24 of a light-shielding film 24, and a part of perimeter of opening 24b (it corresponds to a photodiode 40), respectively, and forms the oblique light reflector, respectively. Moreover, between the oblique light reflective film 60 and a light-shielding film 24, while the groove through hole 61 where it filled up with the tungsten along with a part of perimeter of opening 24a is formed, the groove through hole 62 where it filled up with the groove tungsten along with a part of perimeter of opening 24b is formed. The oblique light reflective film 60 and a through hole 61 constitute the

oblique light reflective section formed along with a part of perimeter of opening 24a from a gestalt of this operation. Moreover, the oblique light reflective film 60 and a through hole 62 constitute the oblique light reflective section formed along with a part of perimeter of opening 24b.

[0044] An operation of these oblique light reflective sections is explained in full detail behind.

[0045] Drawing 6 is the circuit diagram showing the solid state camera by the gestalt of this operation which arranged the unit pixel shown in drawing 1 thru/or drawing 5 to the two-dimensional matrix (mxn).

[0046] Each pixel used as a unit pixel so that the explanation about the structure mentioned above may also show Two P channelMOSFET9a over JFET2, the transfer gate 3, the reset gate 5 that exists in [one] 4 or 1 pixel of reset drains, and a contiguity pixel by one half, In order to acquire a video signal, it consists of a photodiode 1 as a light sensing portion for an image pick-up which receives original incident light, and a photodiode 40 as a light sensing portion for the amount monitors of incident light. Furthermore, P channel MOS transistor 9 which consists of the gate fields 15, the reset gates 5, and the reset drains 4 of JFET2 exists in [one] 1 pixel as a switching element which controls the electric

connection and the cutoff between the reset drain 4 and the gate field 15 of JFET2. These are electrically connected, as shown in drawing 5 .

[0047] The source field (S) 14 of each JFET2 is connected in common by the vertical signal line 22-1 - 22-n (equivalent to the vertical signal line 22 in drawing 5) for every train of matrix arrangement, respectively.

[0048] The drain field (D) of each JFET2 is connected to the drain power source VDD by the N type epitaxial layer 11 [all / pixel].

[0049] For every line of matrix arrangement, the transfer gate wiring 20-1 - 20-m (equivalent to the transfer gate wiring 20 in drawing 5) connect common to the direction of a horizontal scanning, and the transfer gate 3 is connected to the vertical-scanning circuit 7. And it operates for every line by driving pulse phiTG1 sent out from the vertical-scanning circuit 7 - phiTGm.

[0050] In each line of matrix arrangement, the reset drain 4 and the gate field 15 of JFET2 are arranged by turns at a line writing direction (the direction of a horizontal scanning), gate electrode 5a is altogether arranged between each pixel, and said P channel MOSFET9a is formed. In each line of matrix arrangement in addition, gate electrode 5a between all the reset gates 5 in the pixel of the line concerned and the pixel of the line concerned The reset gate

wiring 21 connects common to a line writing direction for every line altogether. By driving pulse phiRSG1 sent out from the vertical-scanning circuit 7 - phiRSGm, it will operate for every line and P channel MOSFETs 9 and 9a as a switching element of the line concerned will be altogether turned on and off to coincidence.

[0051] For this reason, since the reset drain wiring 24 is electrically connected to the reset drain 4 of any one or more horizontal pixels for every line, so that drawing 6 may also show When all MOSFETs 9 and 9a of the line concerned turn on for every line (it is in switch-on) The gate field 15 and the reset drain 4 of JFET2 of the line concerned will be in the condition of having connected electrically to the reset drain wiring 24 of the line concerned. [of all pixels] The gate field 15 and the reset drain 4 of all JFET(s)2 of the line concerned are electrically connected by P channel MOSFET9a between pixels. Therefore, it will be in the condition of having connected electrically to the reset drain wiring 24 of the line concerned also about the gate field 15 of JFET2 of a pixel where the reset drain 4 is not directly connected to the reset drain wiring 24. Moreover, when all MOSFETs 9 and 9a of the line concerned turn off for every line (it is in a cut off state), the gate field 15 of JFET2 of all the pixels of the line concerned will

be in the condition of having been electrically intercepted to the reset drain wiring 24 of the line concerned.

[0052] Therefore, for every line, while making the reset drain wiring 24 of the line concerned discharge the charge of the gate field 15 of JFET2, this signal can be given to the gate field 15 of JFET2 of all the pixels of the line concerned by giving driving signal phiRSD for controlling the potential of the gate field 15 concerned.

[0053] moreover, about each line, when all P channel MOSFETs 9 and 9a of the line concerned turn on Since the gate field 15 and the reset drain 4 of all JFET(s)2 of the line concerned are electrically connected by P channel MOSFET9a between pixels, the reset drain 4 of the line concerned It will be in the condition of having connected electrically to the reset drain wiring 24 of the line concerned, via P channelMOSFET9a of the line concerned, and the reset drain 4. Therefore, the photocurrent by the signal charge (this operation gestalt hole) generated according to the light which carried out incidence from said opening 24b can be made to output from the reset drain wiring 24 of the line concerned.

[0054] About each line, the reset drain wiring 24 of each line concerned is

connected to the output section of each driving pulse phiRSD of the line of the vertical-scanning circuit 7 concerned through the switch QA which consists of an MOSFET etc., respectively, respectively, and Switch QB is further connected, respectively between the reset drain 24 of each line concerned, and the quantity of light monitor signal output terminal 50. Driving pulse phiPD is impressed to the gate electrode of each switch QA, and the pulse which reversed driving pulse phiPD at the knot gate 51 is impressed to the gate electrode of each switch QB. The change section which changes the condition that driving signal phiRSD for each of said switch QA and each switch QB to control the potential of the gate field 15 concerned while making the reset drain wiring 24 of each line discharge the charge of the gate field 15 of JFET2 of each pixel of the line concerned is supplied, and the condition make the signal which appeared in the wiring 24 concerned from the reset drain wiring 24 of the line concerned output consists of gestalten of this operation. Therefore, with the gestalt of this operation, the photocurrent Ip generated with the reset drain 4 of each pixel can be outputted to the component exterior from a terminal 50 through Switch QB.

[0055] It connects with a constant current source 26-1 - 26-n in one side, constant current flows from a constant current source 26-1 - 26-n by this, and the

vertical signal line 22-1 - 22-n constitute the source follower circuit from JFET4, and a constant current source 26-1 - 26-n. the output side of this source follower circuit -- respectively -- the difference as a readout circuitry -- it connects with the processing circuit 27-1 - 27-n. difference -- the processing circuit 27-1 - 27-n -- capacity 28-1 - 28- it consists of switches 29-1, such as n and MOSFET, - 29-n. Common connection of the gate of a switch 29-1 - 29-n is made, and it operates by pulse phiN. difference -- the output section of the processing circuit 27-1 - 27-n is connected to the signal output line 34 through the level selecting switch 39-1 - 39-n. the pulse phiH1 - phiHn to which the level selecting switch 39-1 - 39-n are sent out from the horizontal scanning circuit 8 -- operating sequentially -- difference -- the output of the processing circuit 27-1 - 27-n is made to output to the signal output line 34 one by one This output is outputted outside through the output amplifier 35 connected to the signal output line 34. In addition, the output-signal line 34 is grounded through the switch 36. This switch 36 operates by pulse phiRH.

[0056] Next, the actuation timing chart of the shutter of the solid state camera and the camera concerned in the case of picturizing a still picture using the single lens reflex camera digital still camera which carried the solid state camera

by the gestalt of this operation is shown in drawing 7 .

[0057] By period T1a of the first half within a period T1, the transfer gate 3 of all pixels is turned on and off, the charge of the photodiode 1 which are all pixels is transmitted to the gate field 15 of JFET2, and a photodiode 1 is reset. Since each driving pulse phiRSD serves as an electrical potential difference VGH, each driving pulse phiRSG serves as a low level and P channel MOSFETs 9 and 9a are altogether turned on at this time, the gate field 15 of JFET2 is set as the electrical potential difference VGH.

[0058] Next, by period T1b of the second half within a period T1, each driving pulse phiRSD is made high-level, also at this time, since P channel MOSFETs 9 and 9a are turned on altogether, the gate field 15 of JFET2 of all pixels is set as an electrical potential difference VGL (potential which makes JFET4 turn off), initialization of a pixel is completed, and preparation included in an exposure condition is completed.

[0059] In a period T2, a shutter 101 opens and it will be in an exposure condition. P channel MOSFETs 9 and 9a of the line containing said 1st pixel which has the function which carries out the monitor of the quantity of light at this time are turned on altogether, and it has changed to the condition that the reset drain

wiring 24 was connected to the output terminal 50 since pulse phiPD was a low level, Switch QB turned on and Switching QA turned off. Consequently, the photocurrent Ip generated in each pixel flows to the photocurrent integrating circuit (not shown) of a shutter control circuit, and the output voltage Vip changes, as shown in drawing 7 . Since the inclination of an electrical potential difference Vip is proportional to the incident light reinforcement to a solid state camera 15, when it carries out the monitor of the electrical potential difference Vip, while exposing desired light exposure, it can ask on real time. That is, when the output voltage Vip of a photocurrent integrating circuit exceeds reference voltage Vc by drawing 7 , a delivery shutter is closed for a control signal from a shutter control circuit. Then, each line is read one by one.

[0060] Since Switch QB turns off and Switching QA turns on by period T3, the reset drain wiring 24 has changed to the vertical-scanning circuit 7 side. Since P channel MOSFETs 9 and 9a are altogether turned on at this time, the gate field 15 of JFET2 is set as an electrical potential difference VGH, and after that, P channel MOSFETs 9 and 9a turn it off, and it is made floating by driving pulse phiRSD of the line concerned.

[0061] by period T four, a signal carries out reading appearance from the source

field 14 of JFET2 in source follower mode -- having -- as a reference signal (dark output) Vref -- difference -- it is held at the capacity 28 of the processing circuit 27. And if pulse phiN becomes a low and a switch 29 turns off, the output side (29 sides) of capacity 28 will become floating.

[0062] In a period T5, the lightwave signal charge accumulated in the photodiode 1 is transmitted to the gate field 15 of JFET2 through the transfer gate 3. Since the output side of capacity 28 is floating at this time, difference signal Vs-Vref of a lightwave signal (bright output) Vs and a reference signal (dark output) Vref by which reading appearance was carried out from the source field 14 of JFET2 (S) appears.

[0063] In a period T6, the level selecting switch 39 carries out sequential ON by the horizontal scanning circuit 8, reading appearance of difference signal Vs-Vref which is each pixel of the line concerned is carried out from capacity 28-i as a picture signal, and it is outputted from an output terminal OUT through the output amplifier 35.

[0064] Said period T3-T6 are successively repeated about each line.

[0065] Thus, since the solid state camera by the gestalt of this operation can carry out the monitor of the quantity of light which carries out direct incidence to

a solid state camera during exposure on real time, even if the amount of incident light changes, it can be picturized by the always optimal exposure time at the digital still camera using the solid state camera concerned. In addition, about the case where a stroboscope is used, similarly, TTL modulated light can be carried out and it can picturize by the optimal exposure time.

[0066] Here, the solid state camera as an example of a comparison shown in drawing 8 thru/or drawing 11 is compared and explained about the technical meaning of the oblique light reflective section (the oblique light reflective film 60, through holes 61 and 62) mentioned above.

[0067] Drawing 8 thru/or drawing 11 support drawing 1 thru/or drawing 4 , respectively. In drawing 8 thru/or drawing 11 , the same sign is given to the same as that of the element in drawing 1 thru/or drawing 4 , or a corresponding element, and the overlapping explanation is omitted. The place where the solid state camera shown in drawing 8 thru/or drawing 11 differs from the solid state camera by the gestalt of this operation is only the point that the oblique light reflective section (the oblique light reflective film 60, through holes 61 and 62) is not formed.

[0068] As shown in drawing 9 , while carrying out the monitor of the quantity of

light of the incident light 100 which carried out incidence aslant, will pass through the reset gate 5 which consists of polish recon for oblique-incidence Mitsunari [a part of], it will make an optical generating charge incorrect-mixed to JFET2, and it will become impossible to grasp the amount of incident light to accuracy as a quantity of light monitor in this example of a comparison among the incident light 100 which passed opening 23.

[0069] Moreover, in this example of a comparison, the charge generated by the incident light which passed through the transfer gate 3 which consists of polish recon at the time of the both sides of the between at the time of this photography while carrying out the monitor of the quantity of light, as shown in drawing 10 will incorrect-mix to JFET2. Therefore, while monitor precision falls, the sensibility lowering under this photography will be brought about.

[0070] furthermore, in this example of a comparison, as shown in drawing 11 , like the case of drawing 9 mentioned above For oblique-incidence Mitsunari [a part of] among the light which was going to face carrying out the monitor of the quantity of light, was going to pass opening 24a, and was originally going to carry out incidence to the reset drain 4 Pass the reset gate wiring 21 which consists of polish recon, and the generating charge incorrect-mixes through the

P type lateral overflow drain diffusion layer 6 to the P type charge storage field 12 (field 12 which appeared the left end in drawing 11) of the photodiode 1 of a contiguity pixel. It will become impossible to grasp the amount of incident light to accuracy as a quantity of light monitor. In addition, while the charge generated by the light which passed the transfer gate wiring 20 among the incident light 100 which passed opening 24b and carried out oblique incidence to the photodiode 1, and invaded will incorrect-mix to the reset drain 4 which constitutes a photodiode 40 and making the output as a quantity of light monitor into incorrectness, the sensibility lowering under this photography will be brought about.

[0071] On the other hand, according to the gestalt of this operation, although the situation of drawing 2 and drawing 3 is the same as drawing 9 of the example of a comparison, and the situation of drawing 10 , the situations shown in drawing 4 differ by forming the oblique light reflective section mentioned above as greatly as the situation of drawing 11 of the example of a comparison.

[0072] Namely, according to the gestalt of this operation, as shown in drawing 4 , the reset gate wiring 21 which consists of polish recon among the light which was going to pass opening 24b and was originally going to carry out incidence to the reset drain 4 is passed. The amount of [which the generating charge

incorrect-mixes through the P type lateral overflow drain diffusion layer 6 to the P type charge storage field 12 (field 12 which appeared the left end in drawing 11) of the photodiode 1 of a contiguity pixel in the case of drawing 11] oblique-incidence Mitsunari It is reflected on the side face of the through hole 62 filled up with the side face and tungsten of the oblique light reflective film 60 which consist of aluminum film of the 1st layer, and incidence is carried out to the P type reset drain diffusion layer 4 which should fall essentially. Consequently, incorrect mixing to the P type charge storage field 12 of the photodiode 1 of a contiguity pixel can be controlled, and monitor sensibility and monitor precision can be raised.

[0073] According to the gestalt of this operation, as shown in drawing 4 , it also sets into the part of a photodiode 1. Moreover, similarly The amount of [passed opening 24a in the case of drawing 11 , passed the polish recon transfer gate wiring 20, and the optical generating charge was made to incorrect-mix in to the P type reset drain diffusion 4] oblique-incidence Mitsunari It is reflected on the side face of the through hole 61 filled up with the side face and tungsten of the oblique light reflective film 60 which were formed by aluminum film of the 1st layer, and incidence is carried out to the P type photodiode diffusion 12 which

should fall essentially. Consequently, sensibility can be raised at the time of this photography, without a charge's incorrect-mixing to the reset drain 4 at the time of a quantity of light monitor, and reducing the quantity of light monitor precision at it.

[0074] About the construction material of the oblique light reflective film 60, what has a high reflection factor to incident light is suitable, and although a metal is desirable, it is desirable to consider as the 1st layer aluminum film which uses aluminum as a principal component as well as the wiring layer of the 1st layer like the gestalt of this operation also from the consistency of a process process. You may dissociate with an electrode layer or a wiring layer like the gestalt of this operation, and the oblique light reflective film 60 may be used also [wiring layer / an electrode layer or].

[0075] Moreover, about the clearance between the light-shielding film 24 which is aluminum film of the 2nd layer, and the oblique light reflective film 60 which is aluminum film of the 1st layer, since it becomes the factor of incorrect mixing of oblique-incidence light, it is desirable to control that form the through holes 61 and 62 filled up with the tungsten like the gestalt of this operation, connect, and light carries out incidence to the clearance.

[0076] It is desirable to make it approach so that the circumference of the reset drain 4 which carries out the monitor of the quantity of light may be surrounded like the gestalt of this operation , and to arrange about the arrangement pattern of the oblique light reflective section (the oblique light reflective film 50 , through holes 61 and 62) , when reflecting a part for oblique incidence Mitsunari in the location which should be effectively carried out incidence essentially .

[0077] If arrangement of the oblique light reflective section (the oblique light reflective film 50, through holes 61 and 62) has asymmetry (asymmetry about point symmetry) notably to the core (namely, opening 24b) of the reset drain 4 When the arrangement pattern to the reset drain 4 is made the same in all pixels, The dependency over the location of each pixel in the light-receiving field of a solid state camera arises in the sensibility property of a quantity of light monitor (that is, the quantity of light which reflects in the oblique light reflective section and originally falls to the reset drain 4 by differing according to the location of a pixel). The sensibility properties of a quantity of light monitor differ, and it is not desirable.

[0078] namely, the optical axis of image formation lenses, such as a camera, from being set up near the core of the field (image area) over which the pixel is

distributed While the sense to which the incident light to each pixel inclines maintains symmetry to said core (for example, the core of an image field is received by the right-hand side pixel and the left-hand side pixel) Extent of the inclination from which the direction to which incident light inclines becomes reverse becomes large toward the outside from a core (that is, the inclination of the light which carries out incidence of the pixel of a periphery to this becomes large). for this reason , it be because it become difficult for asymmetry and the relation of a location to affect the reflection effect of the oblique incidence light by the oblique light reflective section , and to predict the amount of incident light in the image pick-up ****** location of a solid state camera to accuracy if asymmetry be in a sensibility property by the component side when make the same the arrangement pattern to the reset drain 4 in all pixels .

[0079] Therefore, when making the same the arrangement pattern of the oblique light reflective section in each pixel, in each pixel, it is desirable like the gestalt of this operation to arrange the oblique light reflective section to point symmetry to the core of opening 24b. A pattern design etc. will become easy if the arrangement pattern of the oblique light reflective section in each pixel is made the same.

[0080] But as it arrangement-pattern-******** and the oblique light reflective section to the core of opening 24b mentioned above, even if it does not adopt arrangement of point symmetry according to the location of the pixel to the core (optical axis of an image formation lens) of image area, dispersion in the sensibility between pixels can be reduced. The example is typically shown in drawing 12 . In drawing 12 , the mass in a grid pattern shows each pixel typically. Moreover, in drawing 12 , O shows the optical axis (core of image area) of the image formation lens (not shown) in space this side, and the arrow head maps and shows the direction of the incident ray to a pixel to the flat surface. And arrangement of the reset drain 4 and the oblique light reflector 60 over opening 24b and this is shown only about four pixels of a periphery as a representative. In this example, the oblique light reflector 60 is arranged only to one side of opening 24b.

[0081] By the way, about the pixel near core O, incident light hardly inclines so that the above explanation may show. Therefore, it is not necessary to necessarily form the oblique light reflective section about the pixel near core O.

[0082] [The gestalt of the 2nd operation]

[0083] Drawing 13 is the outline top view showing typically the unit pixel of the

solid state camera by the gestalt of operation of the 2nd of this invention. Drawing 14 is the outline sectional view which met X9-X10 line in drawing 13 . Drawing 15 is the outline sectional view which met Y9-Y10 line in drawing 13 . Drawing 16 is the outline sectional view which met Y11-Y12 line in drawing 13 . These drawing 13 thru/or drawing 16 supports drawing 8 thru/or drawing 11 which shows said example of a comparison, respectively while they corresponds to drawing 1 thru/or drawing 4 which shows the gestalt of said 1st operation, respectively.

[0084] In drawing 13 thru/or drawing 16 , the same sign is given to the same as that of the element in drawing 1 thru/or drawing 4 , or a corresponding element, and the overlapping explanation is omitted.

[0085] The place where the gestalt of this operation differs from the gestalt of said 1st operation As the oblique light reflective film 50 and through holes 61 and 62 are removed, instead each pixel is shown in drawing 13 , drawing 14 , and drawing 16 the oblique light reflective film 70 which consists of aluminum film of the 1st layer and which carried out signal reading appearance and followed a line (vertical signal line) 22 and one so that the whole perimeter (namely, perimeter of opening 24a) of the reset drain 4 for carrying out the monitor of the

quantity of light may be surrounded It is the point currently formed around reset drain 4 as the oblique light reflective section. Therefore, the oblique light reflective film 70 is used also [line / 22 / which is a wiring layer].

[0086] According to the gestalt of this operation, although the situation of drawing 15 is the same as the situation of drawing 10 of the example of a comparison, the situation shown in drawing 14 and drawing 16 differs from drawing 9 of the example of a comparison mentioned above, and the situation of drawing 11 greatly by forming the oblique light reflective film 70 mentioned above.

[0087] According to the gestalt of this operation, as shown in drawing 14 , the amount of [namely,] oblique-incidence Mitsunari of the incident light which passed opening 24a Without passing through the polish recon reset gate 5, and making an optical generating charge incorrect-mix to JFET2 unlike the case of drawing 9 , it is reflected on the side face of the oblique light reflective film 70 formed by aluminum film of the 1st layer, and incidence is carried out to the reset drain field 4 from which it should fall essentially. Consequently, the sensibility and precision as a quantity of light monitor can be raised.

[0088] Moreover, according to the gestalt of this operation, as shown in drawing

16 , the reset gate wiring 21 which consists of polish recon among the light which is going to pass opening 24b and is originally going to carry out incidence to the reset drain 4 is passed. The amount of [which the generating charge incorrect-mixes through the P type lateral overflow drain diffusion layer 6 to the P type charge storage field 12 (field 12 which appeared the left end in drawing 11) of the photodiode 1 of a contiguity pixel in the case of drawing 11] oblique-incidence Mitsunari It is reflected on the side face of the oblique light reflective film 70 which consists of aluminum film of the 1st layer, and incidence is carried out to the P type reset drain diffusion layer 4 which should fall essentially. Consequently, incorrect mixing to the P type charge storage field 12 of the photodiode 1 of a contiguity pixel can be controlled, and monitor sensibility and monitor precision can be raised.

[0089] According to the gestalt of this operation, as shown in drawing 16 , it also sets into the part of a photodiode 1. Furthermore, similarly The amount of [passed with opening 24a in the case of drawing 11 , passed the polish recon transfer gate wiring 20, and the optical generating charge was made to incorrect-mix in to the P type reset drain diffusion 4] oblique-incidence Mitsunari It is reflected on the side face of the oblique light reflective film 70 formed by

aluminum film of the 1st layer, and incidence is carried out to the P type photodiode diffusion 12 which should fall essentially. Consequently, sensibility can be raised at the time of this photography, without a charge's incorrect-mixing to a reset drain at the time of a quantity of light monitor, and reducing the quantity of light monitor precision at it.

[0090] As mentioned above, although the gestalt of each operation of this invention was explained, this invention is not limited to the gestalt of these operations.

[0091] For example, this invention is also applicable to various solid state cameras, such as CCD, CMOS image sensors, and other magnification mold image sensors. Moreover, this invention is also applicable to the solid state camera which has a single light sensing portion to each pixel.

[0092] In the solid state camera by this invention, since the oblique light reflective section which enclosed the light sensing portion on the whole or selectively is formed between light sensing portion opening and a semi-conductor substrate, the solid state camera with which the light which carried out incidence aslant from opening could be reflected in the light sensing portion, therefore the smear was prevented, and sensibility was increased can

be offered.

[0093] Moreover, when the 2nd photodiode (the 2nd light sensing portion) other than the 1st photodiode (the 1st light sensing portion) for picturizing a photographic subject image is formed in a unit pixel as a quantity of light monitor, the light which carried out incidence aslant from opening can be similarly reflected in the photodiode which should fall essentially, and the cross talk for these 2 pixels can be controlled.

[0094]

[Effect of the Invention] As explained above, according to this invention, the inconvenience accompanying the oblique light which carries out incidence can be reduced.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the outline top view showing typically the unit pixel of the solid state camera by the gestalt of operation of the 1st of this invention.

[Drawing 2] It is the outline sectional view which met X1-X2 line in drawing 1 .

[Drawing 3] It is the outline sectional view which met Y1-Y2 line in drawing 1 .

[Drawing 4] It is the outline sectional view which met Y3-Y4 line in drawing 1 .

[Drawing 5] It is the circuit diagram showing the equal circuit of the unit pixel shown in drawing 1 thru/or drawing 4 .

[Drawing 6] It is the circuit diagram showing the solid state camera by the gestalt of operation of the 1st of this invention.

[Drawing 7] It is the actuation timing chart of a solid state camera and a shutter by the gestalt of operation of the 1st of this invention.

[Drawing 8] It is the outline top view showing typically the unit pixel of the solid state camera by the example of a comparison.

[Drawing 9] It is the outline sectional view which met X5-X6 line in drawing 8 .

[Drawing 10] It is the outline sectional view which met Y5-Y6 line in drawing 8 .

[Drawing 11] It is the outline sectional view which met Y7-Y8 line in drawing 8 .

[Drawing 12] It is drawing showing typically the example of the arrangement pattern of the oblique light reflective section.

[Drawing 13] It is the outline top view showing typically the unit pixel of the solid state camera by the gestalt of operation of the 2nd of this invention.

[Drawing 14] It is the outline sectional view which met X9-X10 line in drawing 13 .

[Drawing 15] It is the outline sectional view which met Y9-Y10 line in drawing 13 .

[Drawing 16] It is the outline sectional view which met Y11-Y12 line in drawing 13 .

[Description of Notations]

1 40 Photodiode (light sensing portion)

2 JFET

3 Transfer Gate

4 Reset Drain

5 Reset Gate

6 Lateral Overflow Drain Diffusion Layer of P Type

7 Vertical-Scanning Circuit

8 Horizontal Scanning Circuit

9 P Channel MOSFET

10 High Concentration N Type Silicon Substrate

11 Low Concentration N Type Epitaxial Layer

12 P Type Photodiode Diffusion Layer

13 N Type Surface Depletion-ized Component Diffusion Layer

14 N Type Source Diffusion Layer of JFET

15 P Type Gate Diffusion Layer of JFET

16 N Type Component Isolation Diffusion Layer

17 N Type Channel Diffusion Layer of JFET

18 Reset Drain Diffusion Layer of P Type

20 Transfer Gate Wiring Which Consists of Polish Recon

21 Reset Gate Wiring by Polish Recon

22 Signal Read-out Wiring by 1st Layer Aluminum

24 Reset Drain Wiring Which Made Light-shielding Film by Two-layer Eye AL Serve Double Purpose

24a, 24b Opening

60 70 Oblique light reflective film

61 62 Through hole

100 Incident Light